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Nixon & Vanderhye PC
1100 North Glebe Rd 8th Floor
Arlington, VA 22201-4714

EXAMINER	
MOORE, IAN N	
ART UNIT	**PAPER NUMBER**
2661	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/662,157	CREEDON ET AL.	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 11 is objected to because of the following informalities: the limitation "...**means for monitoring the two sequences to provide an anticipatory signal indicating that the reading sequence approaches proximity to the writing sequence**..." is recited at lines 17-18, and the identical limitation is repeated in line 19-20. Appropriate correction is required unless the identical limitations are purposely repeated. This office action addresses both set of limitations.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki (U.S. 5,222,108).

Regarding Claims 1 and 6, Suzuki'108 discloses a system for transferring a data stream of data packets (see FIG. 3, Incoming Cell Data, ICD) separated by non-packet words (see FIG. 3, Stuff cells RC), from a first clock domain (see FIG. 3, 1st ATM circuit utilizing WCK, write clock) to a second clock domain (see FIG. 3, 2nd ATM circuit utilizing RCK, read clock), the clock domains having similar but not necessarily identical clock frequencies, said system including:

a receiver means (see FIG. 3, 1st ATM circuit),

a transmitter means (see FIG. 3, 2nd ATM circuit),

an elasticity buffer for receiving the data stream from the receiver means and for providing said data stream to said transmitter means (see FIG. 3, FIFO Buffer 11, receiving WCD from the 1st ATM circuit and providing RCD to 2nd ATM circuit. Also, note that, per FIG. 5, the FIFO buffer 11 can expand up to nth locations in order to store plurality of cells (C_n), and thus, it is an elastic buffer),

means for writing, the data stream into the elasticity buffer in a cyclic sequence under the control of a first clock frequency in a first clock domain (see FIG. 3, WCD and WCK; see col. 2, line 41 to col. 3, line 45; note that WCD are written into the buffer in accordance with WCK),

means for reading the data stream out of the elasticity buffer in a cyclic sequence under the control of a second clock frequency in a second clock domain (see FIG. 3, RCD and RCK; see col. 2, line 41 to col. 3, line 45; note that RCD are read from the buffer in accordance with RCK), said second clock frequency being nominally the same as the first clock frequency (see FIG. 3, WCK, RCK, 1st and 2nd ATM circuits; note that both WCK and RCK would usually be the same since both are being utilized in similar ATM circuits);

means for monitoring the two sequences to provide an anticipatory signal indicating that the reading sequence approaches proximity to the writing sequence (see FIG. 3, Write-in control unit 40, main control unit 12a, and read-out control unit 50; see col. 5, line 45-54, and col. 7, line 55 to col. 8, line 2; note that the control unit observes write-in cell number and

read-out cell number. When writing and reading cell numbers approach immediacy, it supplies the selection signal;)

means in the first clock domain for inserting a non-packet word into said data stream (see FIG. 3, Stuff Cell Data, RC and FIG. 6, Cx; see col. 6, line 62 to col. 7, line 6; note that RC is inserted into the data stream WCD in 1st ATM circuit side.) and

means in the second clock domain for detecting the existence of the inserted non-packet word and for causing the buffer to advance the reading cycle thereby to discard the inserted non-packet word (see FIG. 3, DI and FIG. 8; see col. 7, line 25-55; note that the control unit detects and discards the excess/extra data cell in the 2nd ATM circuit side. The stuff cell data is inserted in 1st ATM circuit side in order to compensate the synchronization, and it is an excess/extra stuff cell at the 2nd ATM circuit side. Thus, when 2nd circuit side experiences any excess/extra data that can cause buffer jitter, the stuffed cell must be discarded in order to compensate the synchronization. Also, per FIG. 8, cell discarding means forwarding/skipping the reading task/cycle to the next cell, or pause reading the current cell and begins reading the next cell).

Regarding Claim 2, Suzuki'108 discloses wherein the inserted non-packet word is an idle byte (see FIG. 3, the stuff data cell). Note that it is well known in the art of synchronization that stuff data is utilized for the purpose synchronizing the clocks. Thus, it is clear that the stuff data cell is the idle cell data/byte.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki'108 in view of well-established teaching in art.

Regarding Claims 3 and 8, Suzuki'108 discloses wherein the elasticity buffer has a maximum of $\mathbf{n}^{th}$ storage locations (see FIG. 5, FIFO 11 and C_n).

Suzuki'108 does not explicitly disclose the elasticity buffer has a maximum of five storage locations.

However, the above-mentioned claimed limitations are well known in the art. In particular, one having ordinary skill in the art can design the elasticity buffer to have a maximum of five storage locations, by equating Suzuki'108 $\mathbf{n}^{th}$ location to 5.

In view of this, having the system of Suzuki'108 and then given the well-established teaching in art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Suzuki'108, by equating N=5, as taught by well-known teaching. The motivation to combine is to obtain the advantages/benefits taught by well-known teaching that such modification would reduce the cost by building/designing a smaller buffer.

4. Claims 4,5, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki'108 in view of Susnow (U.S. 6,594,329).

Regarding Claims 4 and 9, Suzuki'108 discloses all aspects of the claimed invention set forth in the rejection of Claims 1 and 6 as described above, and further teaches the means for writing and the means for reading.

Suzuki'108 does not explicitly disclose a write pointer and a read pointer.

However, the above-mentioned claimed limitations are taught by Susnow'329. In particular, Susnow'329 teaches a write pointer and a read pointer (see FIG. 4, Write Pointer and Read Pointer, and see col. 5, line 16-65).

In view of this, having the system of Suzuki'108 and then given the teaching of Susnow'329, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Suzuki'108, by providing a read and write pointers, as taught by Susnow'329. The motivation to combine is to obtain the advantages/benefits taught by Susnow'329 since Susnow'329 states at col. 2, line 1-9 that such modification would prohibit the buffer from over-flowing or under-flowing of data since the pointers can synchronize the reading and writing processes.

Regarding Claims 5 and 10, the combined system of Suzuki'108 and Susnow'329 discloses all aspects of the claimed invention set forth in the rejection of Claims 1, 4, 6 and 9 as described above, and further teaches the means for monitoring.

Suzuki'108 does not explicitly disclose a slip detector responsive to the write and read pointers.

However, the above-mentioned claimed limitations are taught by Susnow'329. In particular, Susnow'329 teaches a slip detector responsive to the write and read pointers (see FIG. 4, the combined system of Synchronization Unit 340 and output control unit which controls/synchronizes the Write Pointer and Read Pointer via pointer generation units and control units, and see col. 5, line 16-65).

In view of this, having the system of Suzuki'108 and then given the teaching of Susnow'329, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Suzuki'108, by providing the combined system of Synchronization Unit 340 and output control unit to detect the slips, as taught by Susnow'329. The motivation to combine is to obtain the advantages/benefits taught by Susnow'329 since Susnow'329 states at col. 2, line 1-9 that such modification would prohibit the buffer from over-flowing or under-flowing of data.

5. Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki'108 in view of Findlater (U.S. 6,631,138).

Regarding Claim 7, Suzuki'108 discloses all aspects of the claimed invention set forth in the rejection of Claims 6 as described above, and further teaches the transmitter means having a clock signal source at said first frequency and said receiver means having a clock signal sources at said second frequency (see Suzuki'108 FIG. 5 and FIG.7).

Suzuki'108 does not explicitly disclose the transmitter means is a media access control device having a clock signal source and said receiver means is a physical layer device having second clock signal source.

However, the above-mentioned claimed limitations are taught by Susnow'329. In particular, Findlater'138 teaches the transmitter means is a media access control device having a clock signal source (see FIG. 2, MAC chip with transmit clock) and said receiver means is a physical layer device having second clock signal source (see FIG. 2, PHY chip with receive clock, and see col. 1, line 42-67).

Moreover, Suzuki'108 teaches synchronizing between two clock systems. Findlater'138 teaches two clocks systems at MAC and PHY devices. Thus, Suzuki'108's system can be implemented in Findlater'138 devices in order to synchronize two asynchronous devices. In view of this, having the system of Suzuki'108 and then given the teaching of Findlater'138, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Suzuki'108 by synchronizing between MAC chip (with transmit clock) and PHY chip (with receive clock), as taught by Findlater'138. The motivation to combine is to obtain the advantages/benefits taught by Suzuki'108 since Suzuki'108 states at col. 2, line 28-65 that by implementing synchronization of data transmission phases between two clock systems would minimize the extension fault.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki'108 in view of Satou (U.S. 5,822,327).

Regarding Claim 11, Suzuki'108 discloses a system for transferring a data stream of data packets (see FIG. 3, Incoming Cell Data, ICD) separated by non-packet words (see FIG. 3, Stuff cells RC), said system including:

a receiver means (see FIG. 3, 1st ATM circuit),

a transmitter means (see FIG. 3, 2nd ATM circuit),

an elasticity buffer for receiving the data stream from the receiver means and for providing said data stream to said transmitter means (see FIG. 3, FIFO Buffer 11, receiving WCD from the 1st ATM circuit and providing RCD to 2nd ATM circuit. Also, note that, per FIG. 5, the FIFO buffer 11 can expand up to nth locations in order to store plurality of cells (C_n), and thus, it is an elastic buffer),

to means for writing the data stream into the elasticity buffer in a cyclic sequence under the control of a first clock frequency in a first clock domain (see FIG. 3, WCD and WCK; see col. 2, line 41 to col. 3, line 45; note that WCD are written into the buffer in accordance with WCK),

means for reading the data stream out of the elasticity buffer in a cyclic sequence under the control of a second clock frequency in a second clock domain, said second clock frequency being nominally the same as the first clock frequency (see FIG. 3, RCD and RCK; see col. 2, line 41 to col. 3, line 45; note that RCD are read from the buffer in accordance with RCK), said second clock frequency being nominally the same as the first clock frequency (see FIG. 3, WCK, RCK, 1st and 2nd ATM circuits; note that both WCK and RCK would usually be the same since both are being utilized in similar ATM circuits);

means for monitoring the two sequences to provide an anticipatory signal indicating that the reading sequence approaches proximity to the writing sequence (see FIG. 3, Write-in control unit 40, main control unit 12a, and read-out control unit 50; see col. 5, line 45-54, and col. 7, line 55 to col. 8, line 2; note that the control unit observes write-in cell number and

read-out cell number. When writing and reading cell numbers approach immediacy, it supplies the selection signal);

means for monitoring the two sequences to provide an anticipatory signal indicating that the reading sequence approaches proximity to the writing sequence (same as above),

means to insert a non-packet word into said data stream in the first clock domain (see FIG. 3, Stuff Cell Data, RC and FIG. 6, Cx; see col. 6, line 62 to col. 7, line 6; note that RC is inserted into the data stream WCD in 1st ATM circuit side); and

means in the second clock domain for detecting the existence of the inserted non packet word and for causing the buffer to advance the reading cycle thereby to discard the said inserted non-packet word (see FIG. 3, DI and FIG. 8; see col. 7, line 25-55; note that the control unit detects and discards the excess/extra data cell in the 2nd ATM circuit side. The stuff cell data is inserted in 1st ATM circuit side in order to compensate the synchronization, and it is an excess/extra stuff cell at the 2nd ATM circuit side. Thus, when 2nd circuit side experiences any excess/extra data that can cause buffer jitter, the stuff cell must be discarded in order to compensate the synchronization. Also, per FIG. 8, cell discarding means forwarding/skipping the reading task/cycle to the next cell, or pause reading the current cell and begins reading the next cell).

Suzuki'108 does not explicitly disclose means for performing synchronization tasks in responsive to said anticipatory signal in the first clock domain.

However, the above-mentioned claimed limitations are taught by Satou'327. In particular, Satou'327 teaches means for performing synchronization tasks in responsive to said anticipatory signal in the first clock domain (see FIG. 1, Clock Compares control unit 17

sending feed back control signal Cw to Write clock generator 15 in order to inhibit the write clock from being generated. Thus, it creates/inserts the idle data by idling, and the writing sequence is not incremented, thereby achieving synchronization; col. 4, line 10-30).

In view of this, having the system of Suzuki'108 and then given the teaching of Satou'327, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Suzuki'108, by providing a mechanism to send control signal to the write/first clock side in order to perform synchronization, as taught by Satou'327. The motivation to combine is to obtain the advantages/benefits taught by Satou'327 since Satou'327 states at col. 1, line 45-67 that such modification would minimize the delay ascribable to transmission rate conversion between two clock generators.

7. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki'108 in view of well-established teaching in art.

Regarding Claims 12 and 13, Suzuki'108 a buffer system for transferring a data stream essentially consisting of a succession of data words (see FIG. 3, Incoming Cell Data, ICD from a first clock domain (see FIG. 3, 1st ATM circuit utilizing WCK, write clock) to a second clock domain (see FIG. 3, 2nd ATM circuit utilizing RCK, read clock), said system comprising:

an elasticity buffer having a maximum of $\mathbf{n}^{th}$ storage locations whereby the buffer can store a maximum of $\mathbf{n}^{th}$ data words (see FIG. 5, FIFO 11 and C_n; and FIG. 3, FIFO Buffer 11 receives WCD from the 1st ATM circuit and provides RCD to 2nd ATM circuit. Also, note

that, per FIG. 5, the FIFO buffer 11 can expand up to n^{th} locations in order to store plurality of cells (C_n), and thus, it is an elastic buffer),

means for writing the data stream into the elasticity buffer in a cyclic sequence under the control of the clock frequency in the first clock domain (see FIG. 3, WCD and WCK; see col. 2, line 41 to col. 3, line 45; note that WCD are written into the buffer in accordance with WCK),

means for reading the data stream out of the elasticity buffer in a cyclic sequence under the control of the clock frequency in the second domain (see FIG. 3, RCD and RCK; see col. 2, line 41 to col. 3, line 45; note that RCD are read from the buffer in accordance with RCK); and

means for monitoring the two sequences to provide an anticipatory signal indicating that the reading sequence approaches proximity to the writing sequence (see FIG. 3, Write-in control unit 40, main control unit 12a, and read-out control unit 50; see col. 5, line 45-54, and col. 7, line 55 to col. 8, line 2; note that the control unit observes write-in cell number and read-out cell number. When writing and reading cell numbers approach immediacy, it supplies the selection signal.)

Suzuki'108 does not explicitly disclose an elasticity buffer having a maximum of five storage locations whereby the buffer can store a maximum of five data words, and each of said storage location stores one data byte.

However, the above-mentioned claimed limitations are well known in the art. In particular, one having ordinary skill in the art can design the elasticity buffer to have a maximum of five storage locations whereby the buffer can store a maximum of five data

words, by equating Suzuki'108 $\mathbf{n^{th}}$ location to 5 and modify/assign each storage location to store one data byte instead of one data cell.

In view of this, having the system of Suzuki'108 and then given the well-established teaching in art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Suzuki'108, by equating N=5 and modify one data byte for each storage location, as taught by well-known teaching. The motivation to combine is to obtain the advantages/benefits taught by well-known teaching that such modification would reduce the cost by building/designing a smaller buffer.

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki'108 and well established teaching as stated in Claim 12 above, and further in view of Susnow (U.S. 6,594,329).

Regarding Claim 14, the combined system of Suzuki'108 and well-established teaching in art discloses all aspects of the claimed invention set forth in the rejection of Claim 12 as described above, and further teaches the means for writing, means for reading, and means for monitoring.

Suzuki'108 does not explicitly disclose a write pointer, a read pointer, and a slip detector responsive to the write and read pointers

However, the above-mentioned claimed limitations are taught by Susnow'329. In particular, Susnow'329 teaches a write pointer, a read pointer (see FIG. 4, Write Pointer and Read Pointer, and see col. 5, line 16-65), and a slip detector responsive to the write and read pointers (see FIG. 4, the combined system of Synchronization Unit 340 and output control

unit which controls/synchronizes the Write Pointer and Read Pointer via pointer generation units and control units, and see col. 5, line 16-65).

In view of this, having the combined system of Suzuki'108 and well-established teaching in art, then given the teaching of Susnow'329, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Suzuki'108, by providing a read, write pointers, and the combined system of Synchronization Unit 340 and output control unit to detect the synchronization slips, as taught by Susnow'329. The motivation to combine is to obtain the advantages/benefits taught by Susnow'329 since Susnow'329 states at col. 2, line 1-9 that such modification would prohibit the buffer from over-flowing or under-flowing of data since the pointers can synchronize the reading and writing processes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 703-605-1531. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 703-305-4798. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Ian N Moore
Examiner
Art Unit 2661

INM
1/16/04

RICKY NGO
PRIMARY EXAMINER